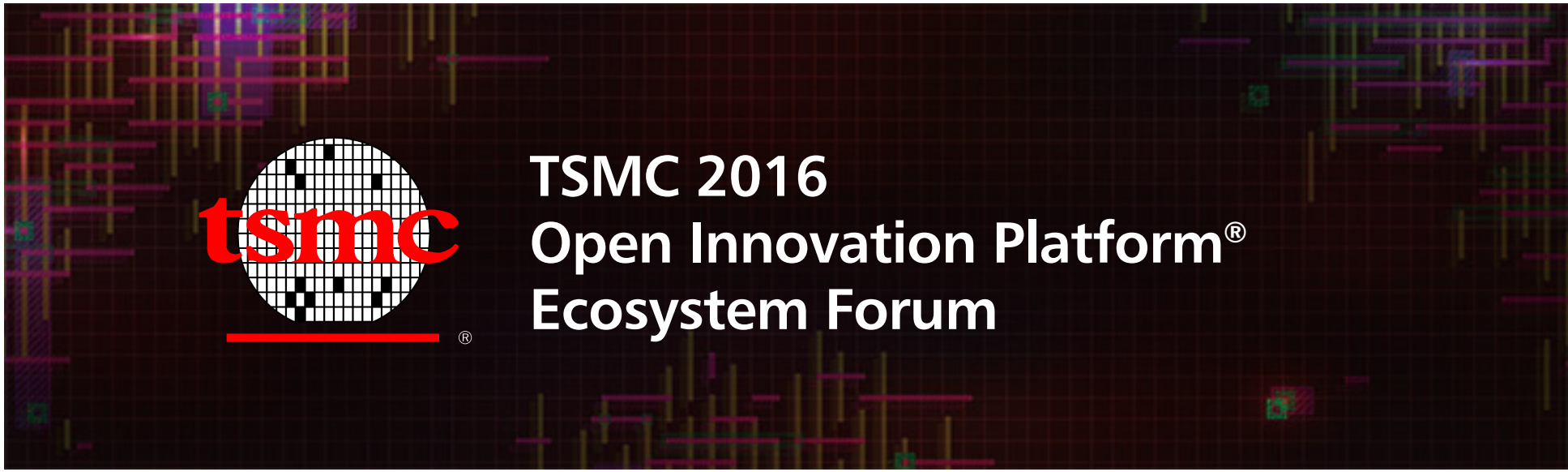
Logic Design Co-Optimization

AMD



ABSTRACT

Design investment and product costs are increasing exponentially with process technology scaling. Early foundry engagement and co-optimization of process, CAD, std cells and design architecture are critical to maximize product performance and minimize unit cost. This presentation shows how a test logic block is used to optimize five key metrics: speed, area, power, yield, and wafer complexity. The test logic block involves running Synthesis, Place and Route. The process enables decisions that co-optimize Foundry process, EDA tools, IP and their interactions. Results show benefits to metal stack, std cell architecture, router, and design architecture.